





# Challenges and New Opportunities in Nanoscale Synthesis and Integration

**CINT Workshop** 

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# Challenges and New Opportunities in Nanoscale Synthesis and Integration

Where will be the CINT focus?

Initially dictated by current strengths?

### Sandia

Microelectronics
Compound Semiconductors
Synthesis, Characterization and Theory

### Los Alamos

Synthesis, Characterization and Theory Biosciences National High Magnetic Field Laboratory Neutron Science Center

## **CINT** Gateway to Sandia

Nanomaterials Microfabrication

## **CINT** Gateway to Los Alamos

Biosciences Nanomaterials

#### Scientific Themes

Nano-Bio-Micro-Interfaces
Nanophotonics and Nanoelectronics
Complex Functional Nanomaterials
Nanomechanics
Theory and Simulation

Large-Scale Synthesis of Pure Single-Walled Carbon Nanotubes with Controllable Properties

(Ultra) Large Scale Integration of Single-Walled Carbon Nanotubes into Electronic, Photonic and Sensor Devices

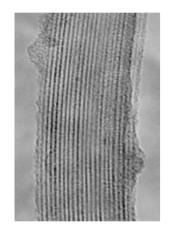
Coherent Integration of Nanomaterial Devices into Neuronal Circuits

Synthesis and Integration of a Room Temperature Superconductor into an Electronic Device

Large-Scale Synthesis of Pure Single-Walled Carbon Nanotubes with Controllable Properties

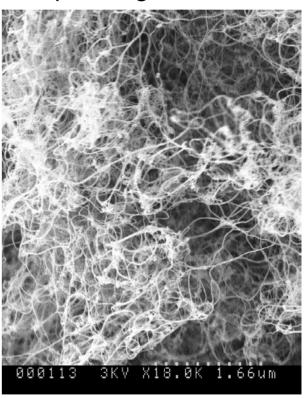
## Single-walled carbon nanotubes (SWNTs)

single cylinder of graphite typical dimensions ⇒ 0.7-1.5 nm diameter, ~ 10 µm length



## SWNTs usually occur in bundles





(Ultra) Large Scale Integration of Single-Walled Carbon Nanotubes into Electronic, Photonic and Sensor Devices

Integration (Self Assembly?)

Interfaces (Interconnects)

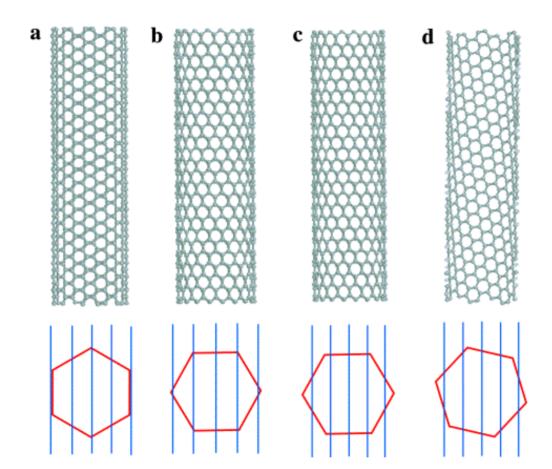
# Novel Approaches to Device Design and Fabrication

The susceptibility of common interconnect metals to electromigration at high current densities (>10<sup>6</sup> A/cm<sup>2</sup>) is a problem.

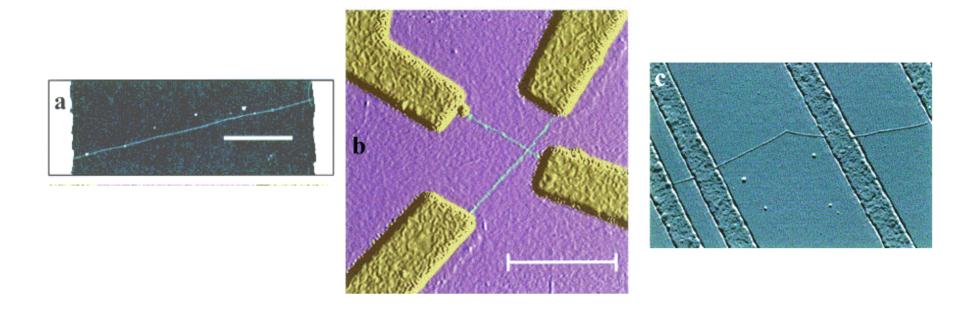
The copper interconnect, introduced in 1998, is now routinely used with minimum feature sizes down to 130 nm. However the electrical resistivity of Cu increases with a decrease in dimensions due to electron surface scattering and grain-boundary scattering. Such size effects arise from interface roughness and small grain size, which are hard to overcome.

The aspect ratio of contact holes for DRAM stacked capacitors now is 12:1 and is expected to increase to 23:1 by 2016. Creating such high aspect ratio contacts with straight walls is an extremely difficult task.

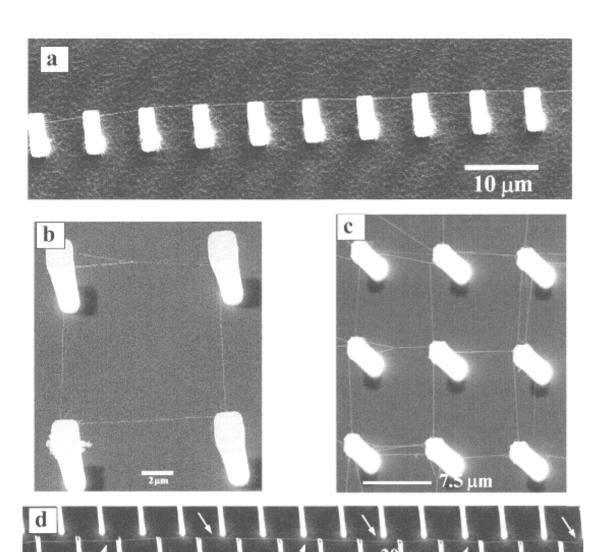
The extraordinary electrical, mechanical, and thermal properties of CNTs may provide near-term solutions for problems in interconnects, chip cooling, etc. in silicon IC technology.



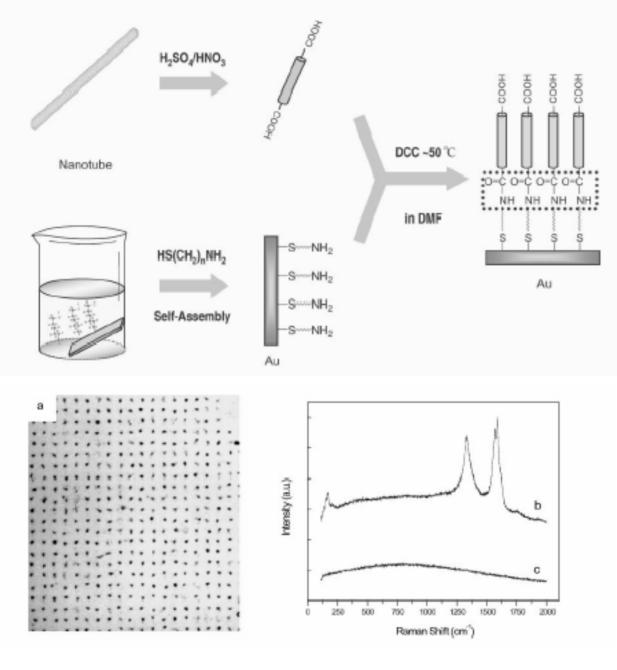
Schematic structures of SWNTs and how they determine the electronic properties of the nanotubes. (a) A (10,10) arm-chair nanotube. Bottom panel: the hexagon represents the first Broulloin zone of a graphene sheet in reciprocal space. The vertical lines represent the electronic states of the nanotube. The center-line crosses two corners of the hexagon, resulting in a metallic nanotube. (b) A (12, 0) zigzag nanotube. The electronic states cross the hexagon corners, but a small band gap can develop due to the curvature of the nanotube. (c) The (14, 0) zigzag tube is semiconducting because the states on the vertical lines miss the corner points of the hexagon. (d) A (7, 16) tube is semiconducting. This figure illustrates the extreme sensitivity of nanotube electronic structures to the diameter and chirality of nanotubes.



Connecting SWNTs to the macroscopic world for electrical measurements. (a) AFM image of a SWNT contacted by metal electrodes (bright regions at the left and right of the image). (b) AFM image of two crossing nanotubes each connected to two metal electrodes (courtesy of Dr. P. McEuen). (c) AFM image of a nanotube heterojunction formed by a metallic tube connected to a semiconducting tube (courtesy of Drs. C. Dekker and Z. Yao).



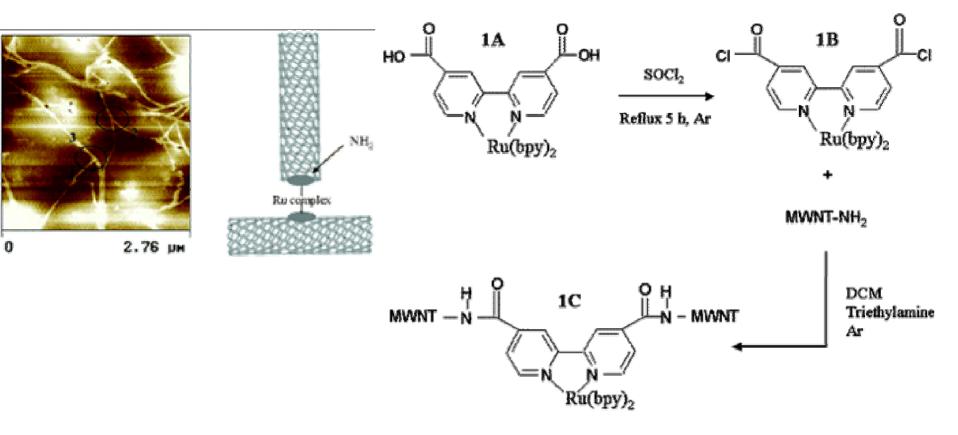
`Self-directed' growth of suspended SWNTs. (a) SEM image of suspended SWNT 'power-line' grown on a row of silicon pillars (bright postlike objects). The line-like structures bridging the posts are SWNTs. (b) A square of suspended SWNT. (c) A square network of suspended SWNTs. (d) A long SWNT bridging many silicon pillars. These results demonstrate that ordered networks of SWNTs can be obtained by self-assembled nanotube growth, which could be utilized for building interesting circuits/devices of nanotubes



Schematic illustration of the surface condensation reaction method for fabricating highly aligned single-walled carbon nanotubes on gold.

Optical microscope image (10 £ 100) of the patterned nanotube assembly on gold, where the dark dot regions are covered with nanotubes (a). Raman spectra of the patterned nanotube assembly on gold taken at the dark spot (b) and at the blank area (c), respectively.

Liu, Z., etal, J. Colloid and Interface Science, 245(2), 311-318



Interconnecting Carbon Nanotubes with an Inorganic Metal Complex

(Ultra) Large Scale Integration of Single-Walled Carbon Nanotubes into Electronic, Photonic and Sensor Devices

Integration (Self Assembly?)

Interfaces (Interconnects)

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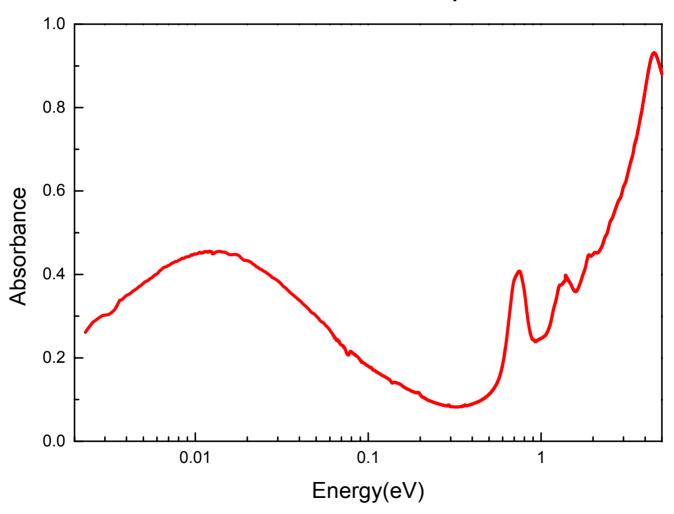
Insulator

Semiconductor

Metal

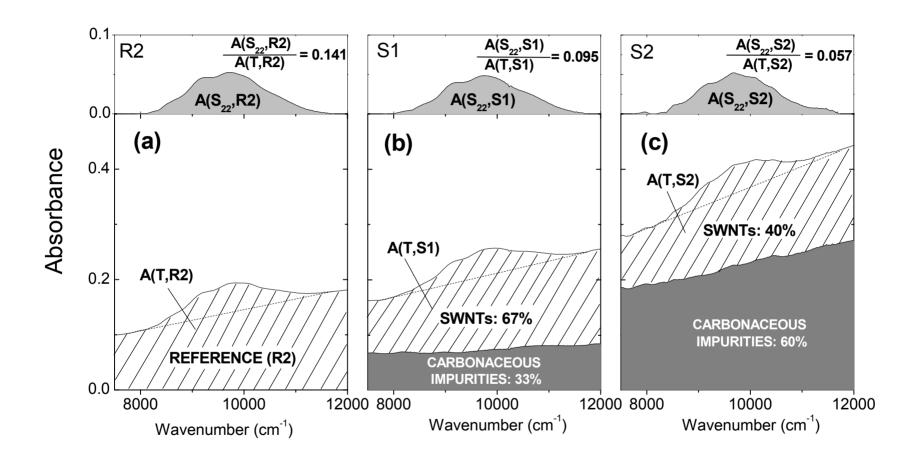
Superconductor

### **SWNT FIR-NIR-Vis-UV Spectrum**



M. E. Itkis, et al. Nano Lett, 2, 155 (2002)

### Purity Evaluation of As-Prepared SWNT Soot



M. E. Itkis, et al. Nano Lett, **3**, 309 (2003)

### C<sub>60</sub> thin film transistors

R. C. Haddon, A. S. Perel, R. C. Morris, T. T. M. Palstra, A. F. Hebard, and R. M. Fleming

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(Received 3 March 1995; accepted for publication 11 May 1995)

N-channel field effect transistors with excellent device characteristics have been fabricated by utilizing  $C_{60}$  as the active element. Measurements on  $C_{60}$  thin films in ultrahigh vacuum show on-off ratios as high as  $10^6$  and field effect mobilities up to  $0.08\,$  cm<sup>2</sup>/V s. © 1995 American Institute of Physics.

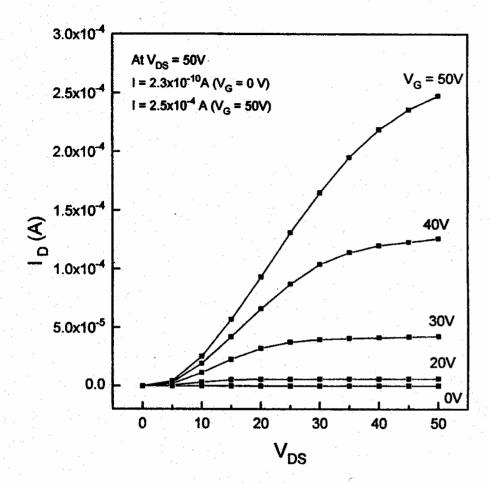


FIG. 1. Drain current  $(I_D)$  vs drain-source voltage  $(V_{DS})$  for various gate voltages  $(V_G)$ , for a  $C_{60}$  thin film transistor.

1/3/\$6.00 © 1995 American Institute of Physics

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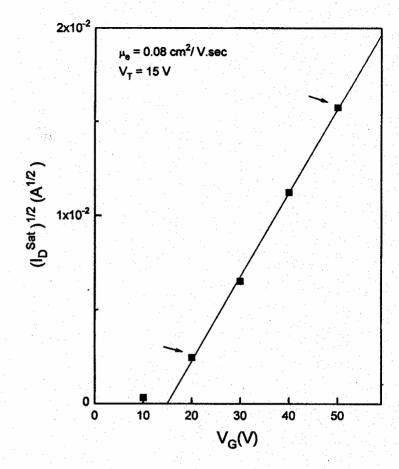


FIG. 2. Plot of the square root of the saturation current at the drain vs gate voltage (data from Fig. 1), together with the derived field effect electron mobility  $(\mu_e)$  and threshold voltage  $(V_T)$ .

$$I_D^{\text{sat}} = \mu \left( \frac{CW}{2L} \right) (V_G - V_T)^2,$$

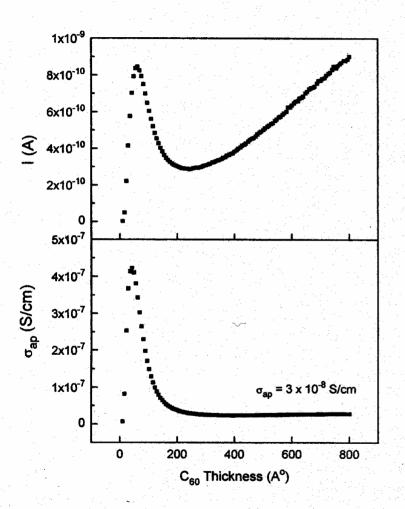


FIG. 3. (a) Drain-source current measured at 10 V, during the deposition of  $C_{60}$  on a thin film transistor. (b) Apparent conductivity ( $\sigma_{ap}$ ), as a function of  $C_{60}$  film thickness (see text).

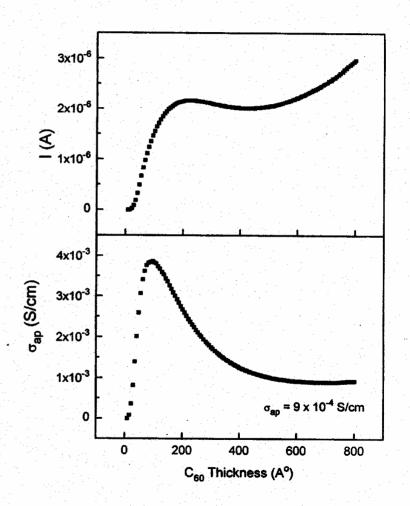
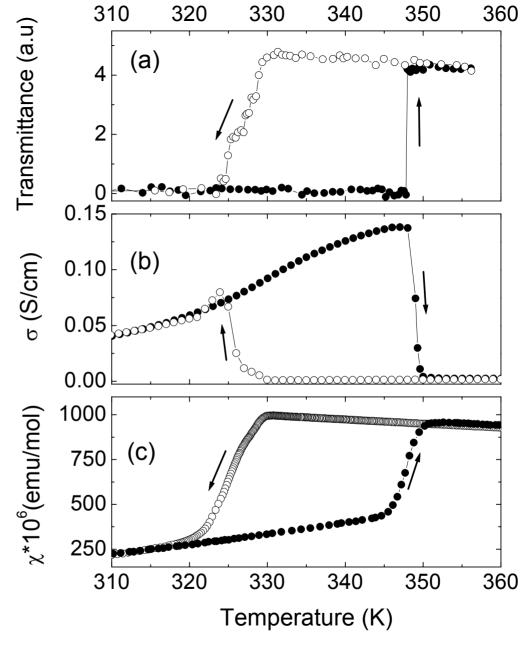


FIG. 4. (a) Drain-source current measured at 1 V, during the deposition of  $C_{60}$  on a thin film transistor that had been treated with TDAE. (b) Apparent conductivity ( $\sigma_{ap}$ ), as a function of  $C_{60}$  film thickness (see text).

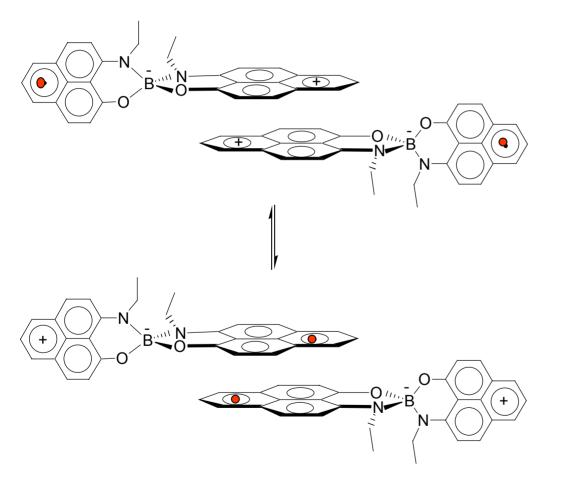
Bistability in Optics,
Conductance and
Magnetism



M. E. Itkis, et al. Science, **296**, 1443 (2002)

Fig.3. Bistability in a) infrared transmittance T at wavelength 3.85  $\mu$ m; b) conductivity  $\sigma$  and c) magnetic susceptibility  $\chi$  due to hysteretic phase transition in butyl radical.

# Mechanism of Phase Transition: Electron Switching



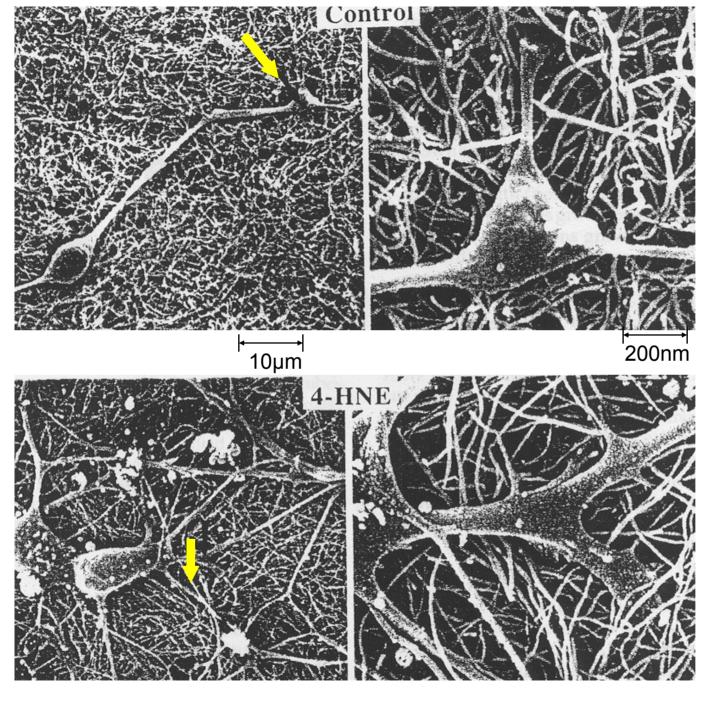
High Temperature State

- Paramagnetic
- Insulating
- •IR-Transparent

Low Temperature State

- Diamagnetic
- Conducting
- •IR-Opaque

Coherent Integration of Nanomaterial Devices into Neuronal Circuits



Neurite growth and branching is enhanced in neurons growing on nanotubes coated with 4-HNE. SEM micrographs showing neurons that had grown for 3 days on unmodified control nanotubes (upper) and nanotubes coated with 4-HNE (lower).

[M.P. Mattson, R.C.Haddon, A.M. Rao, *J.Mol.Neur*. **14**, 175-182, 2000].